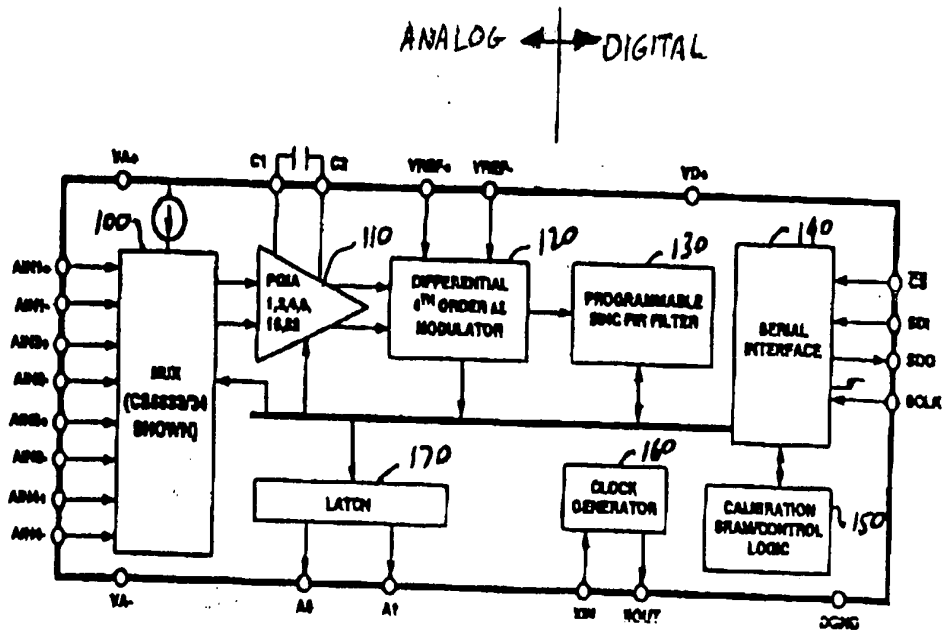

ANALOG
DIGITAL
VA+
C1
C2
VREF+
VREF-
VD+
100
110
120
130
140
MUX
(CS5533/34 SHOWN)
PGIA
1,2,4,8
16,32
DIFFERENTIAL
6TH ORDER ΔΣ
MODULATOR
PROGRAMMABLE
SINC FIR FILTER
SERIAL
INTERFACE
CS
SDI
SDO
SCLK
170
LATCH
160
CLOCK
GENERATOR
CALIBRATION
SRAM/CONTROL
LOGIC
150
VA-
A0
A1
XIN
XOUT
DGND

FIGURE 1.1

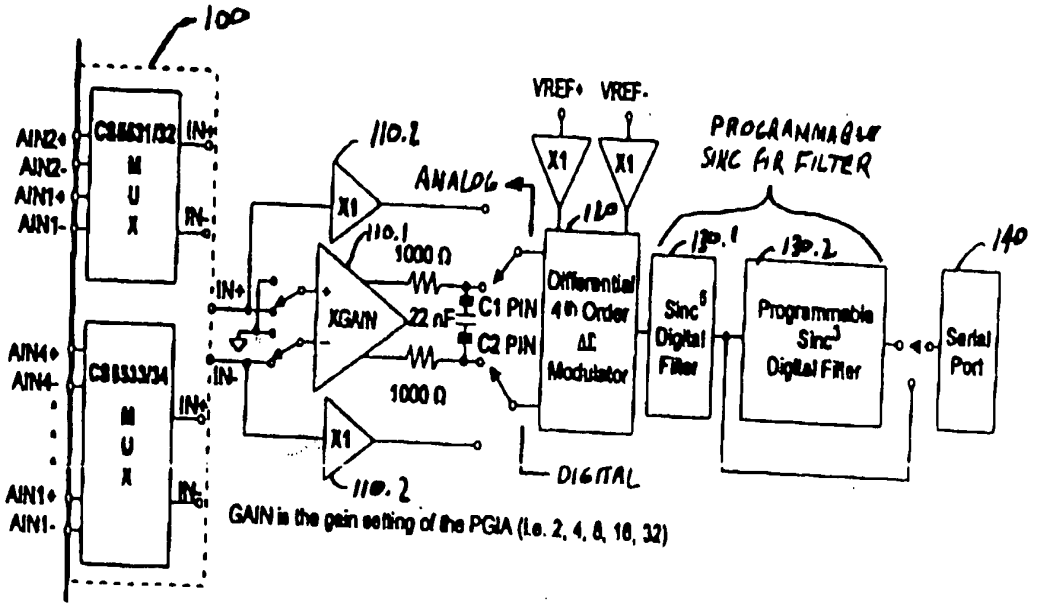

100
AIN2+
AIN2-
AIN1+
AIN1-
MUX
IN+
IN-
AIN4+
AIN4-
AIN1+
AIN1-
110.2
X1
ANALOG
VREF+
VREF-
PROGRAMMABLE
SINC FIR FILTER
110.1
1000 Ω
XGAIN
22 nF
C1 PIN
C2 PIN
1000 Ω
110
Differential
4th Order
ΔΣ
Modulator
Sinc6
Digital
Filter
130.1
Programmable
Sinc3
Digital Filter
130.2
140
Serial
Port
DIGITAL
110.2
GAIN is the gain setting of the PGIA (i.e. 2, 4, 8, 16, 32)

FIGURE 1.2

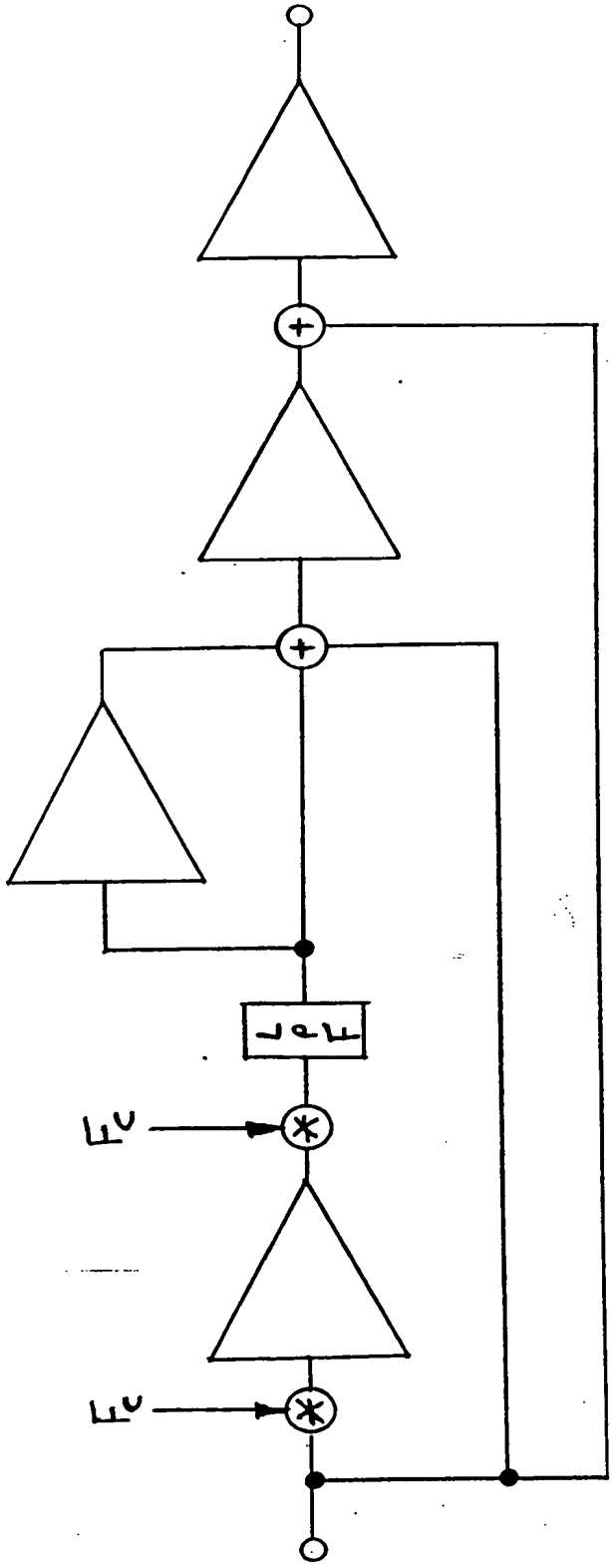


FIGURE 1.3

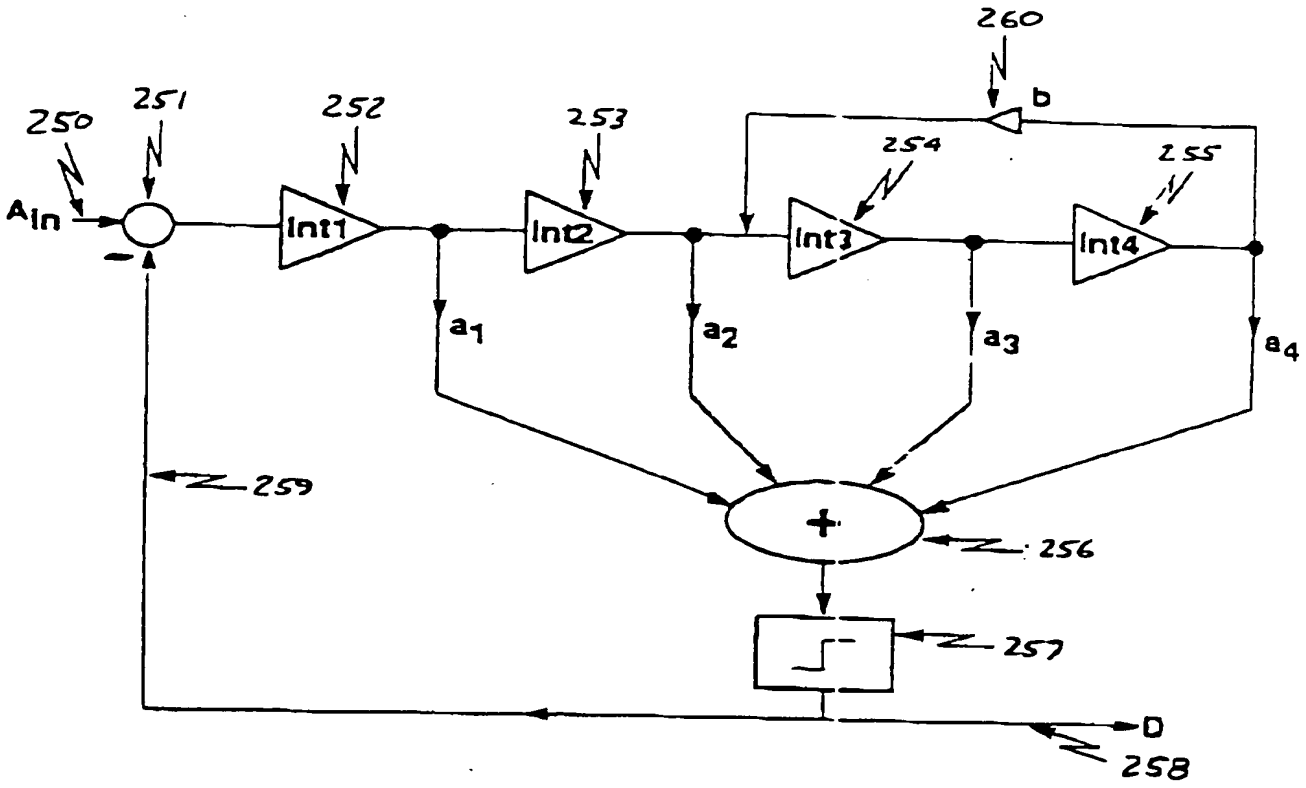

260
b
250
251
252
253
254
255
Ain
Int1
Int2
Int3
Int4
a1
a2
a3
a4
259
+
256
257
D
258

Figure 1.4

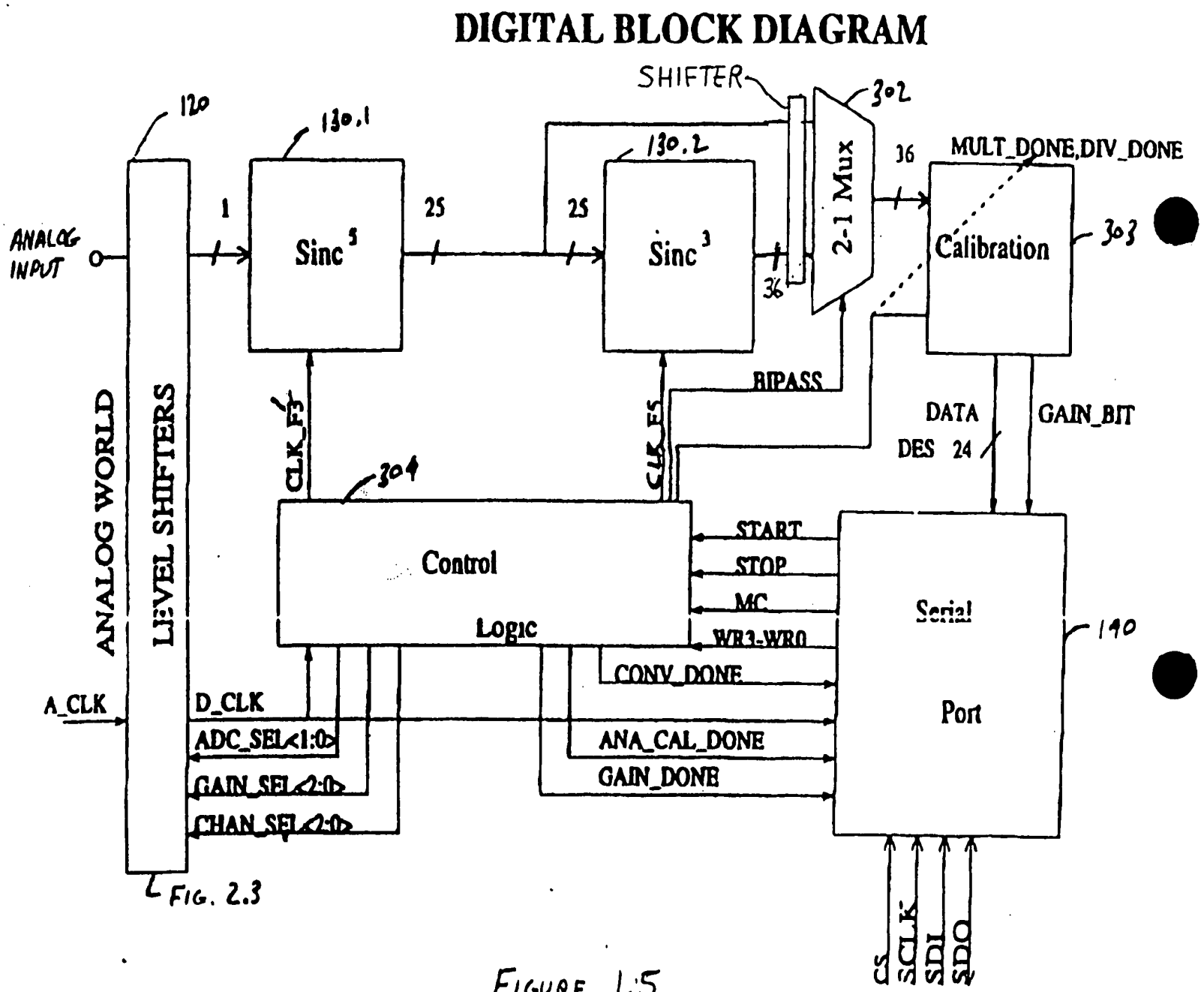


FIG. 2.3

FIGURE 1.5

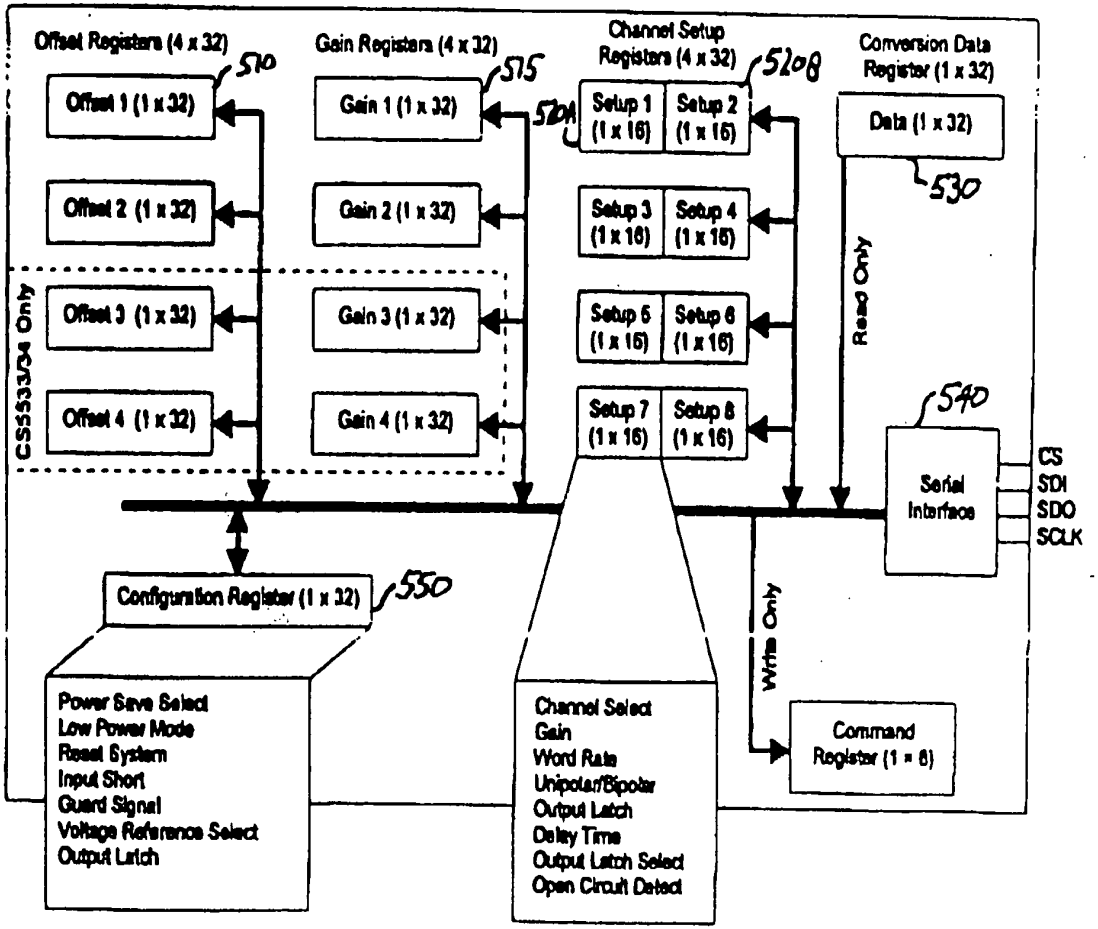

Offset Registers (4 x 32)
510
Gain Registers (4 x 32)
515
Channel Setup Registers (4 x 32)
520B
520A
Conversion Data Register (1 x 32)
Offset 1 (1 x 32)
Offset 2 (1 x 32)
Offset 3 (1 x 32)
Offset 4 (1 x 32)
Gain 1 (1 x 32)
Gain 2 (1 x 32)
Gain 3 (1 x 32)
Gain 4 (1 x 32)
Setup 1 (1 x 16)
Setup 2 (1 x 16)
Setup 3 (1 x 16)
Setup 4 (1 x 16)
Setup 5 (1 x 16)
Setup 6 (1 x 16)
Setup 7 (1 x 16)
Setup 8 (1 x 16)
Data (1 x 32)
530
CS5533/34 Only
Read Only
540
Serial Interface
CS
SDI
SDO
SCLK
Configuration Register (1 x 32)
550
Power Save Select
Low Power Mode
Reset System
Input Short
Guard Signal
Voltage Reference Select
Output Latch
Channel Select
Gain
Word Rate
Unipolar/Bipolar
Output Latch
Delay Time
Output Latch Select
Open Circuit Detect
Write Only
Command Register (1 = 8)

FIGURE 1.6

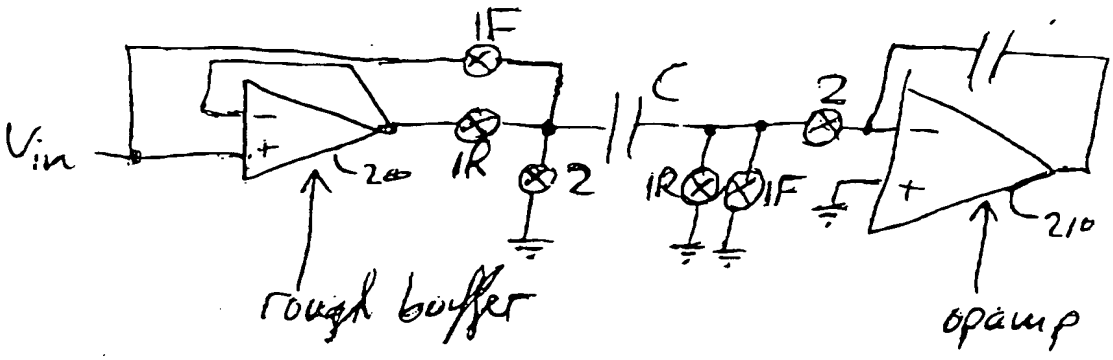


FIGURE 2.0

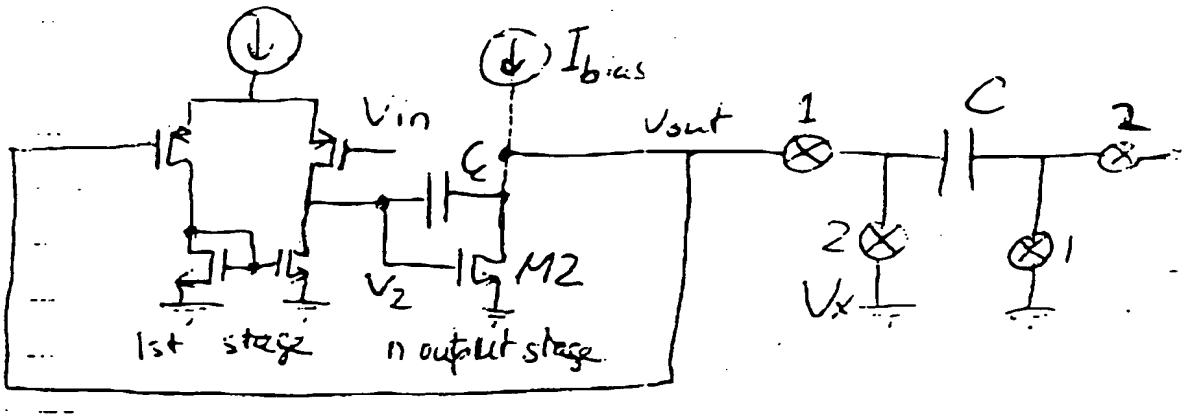


FIGURE 2.1

V_{IN} = CONSTANT

$V_{OUT} > V_X$

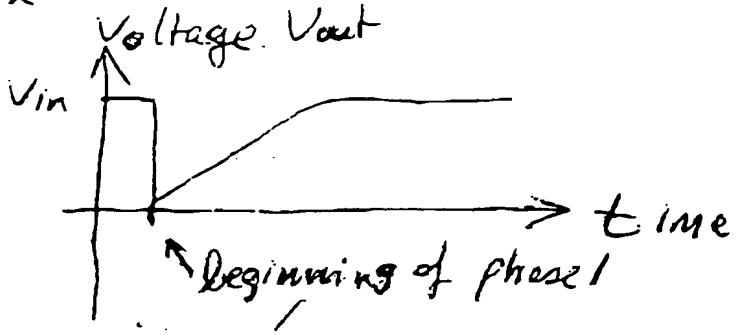


FIGURE 2.2

V_{IN} = CONSTANT

$V_{OUT} < V_X$

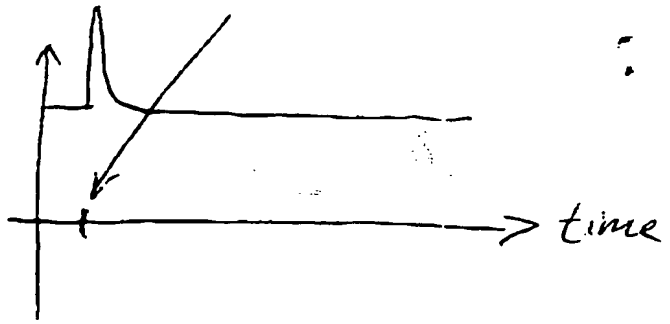


FIGURE 2.3

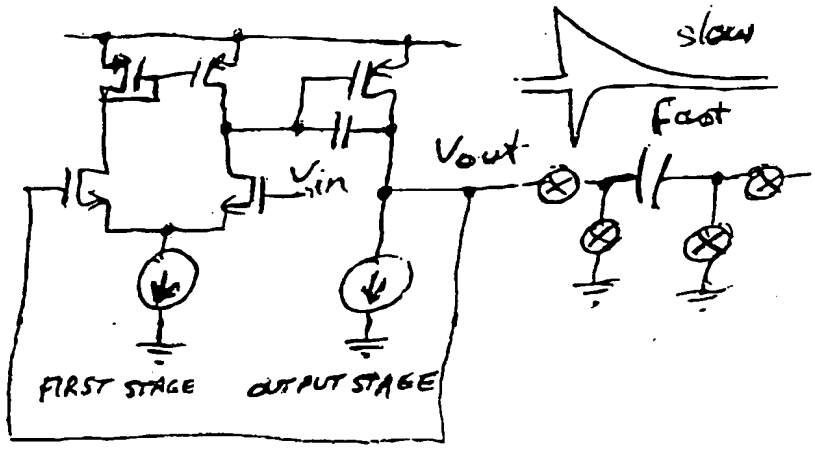


FIGURE 2.4

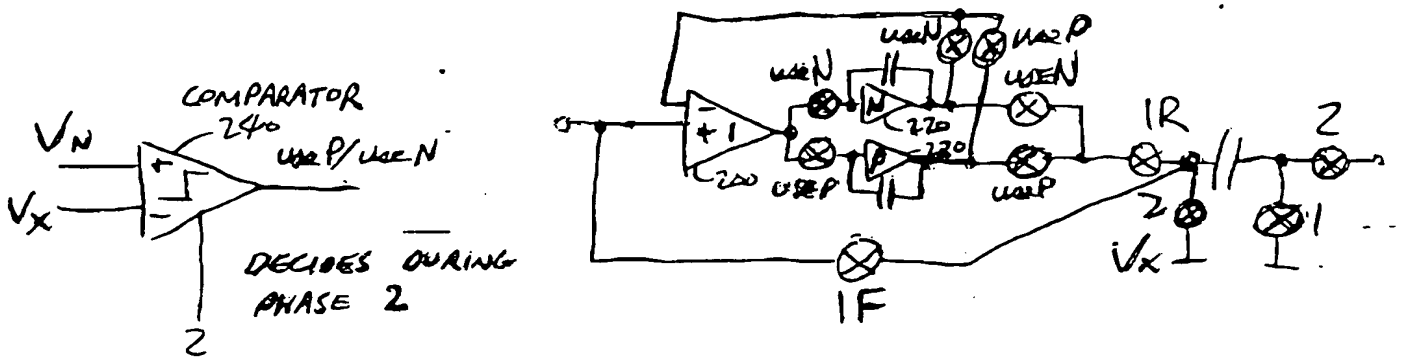
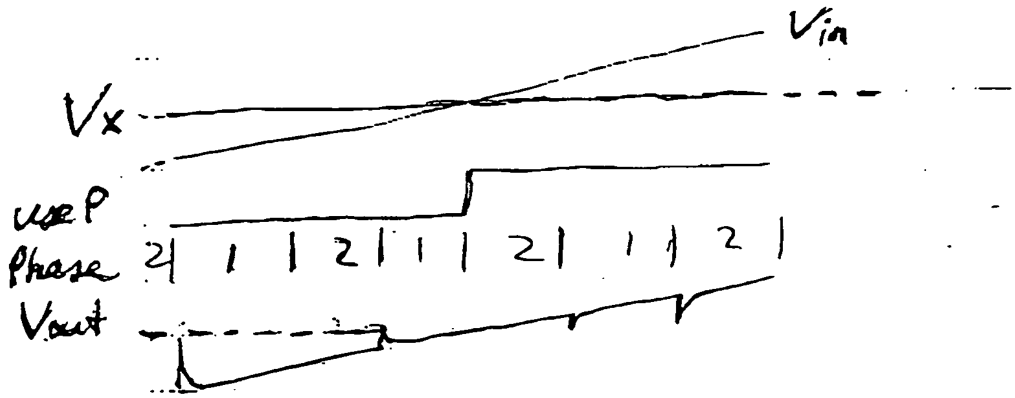

COMPARATOR
240
V_N
V_X
USEP/USEN
DECIDES DURING PHASE 2
2
USEN
USEP
+1
-1
220
230
IR
IF
V_X
2
1

FIGURE 2.5

FIGURE 2.6

FIGURE 2.7

FIGURE 2.8



MULTIPLIER ARCHITECTURE

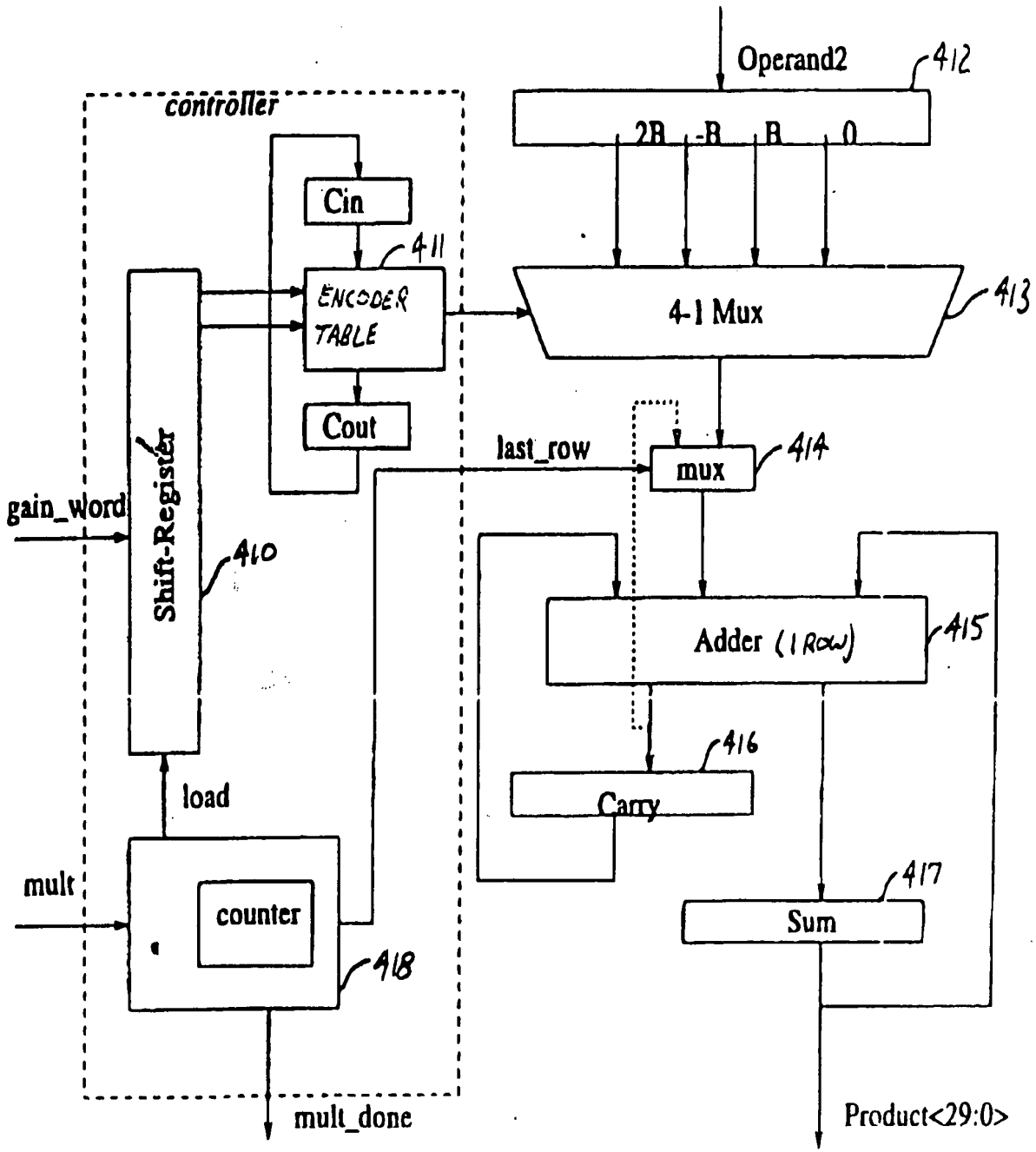


FIGURE 3.1

Multiplication

FIGURE 3.2
(PRIOR ART)

Table 2: Encoding Scheme Proposed

A_{i+1}	A_i	Operation
0	0	$R_i = R_{i-1}/4$
0	1	$R_i = (R_{i-1} + B)/4$
1	0	$R_i = (R_{i-1} + 2B)/4$
1	1	$R_i = (R_{i-1} + 3B)/4$

FIGURE 3.3
(PRIOR ART)

Table 3: Carry Propagate Encoding Scheme

C_{in}	A_{i+1}	A_i	Operation	C_{out}
0	0	0	$R_i = R_{i-1}/4$	0
0	0	1	$R_i = (R_{i-1} + B)/4$	0
0	1	0	$R_i = (R_{i-1} + 2B)/4$	0
0	1	1	$R_i = (R_{i-1} - B)/4$	1
1	0	0	$R_i = (R_{i-1} + B)/4$	0
1	0	1	$R_i = (R_{i-1} + 2B)/4$	0
1	1	0	$R_i = (R_{i-1} - B)/4$	0
1	1	1	$R_i = (R_{i-1})/4$	1

Multiplication

FIGURE 3.4

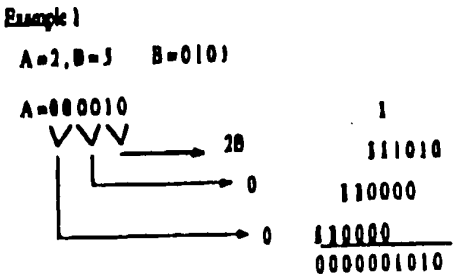
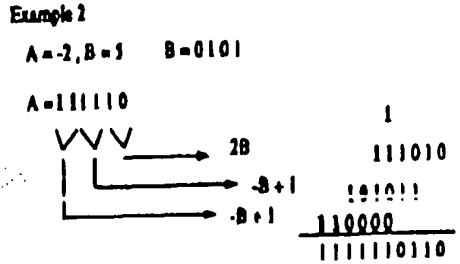


FIGURE 3.5



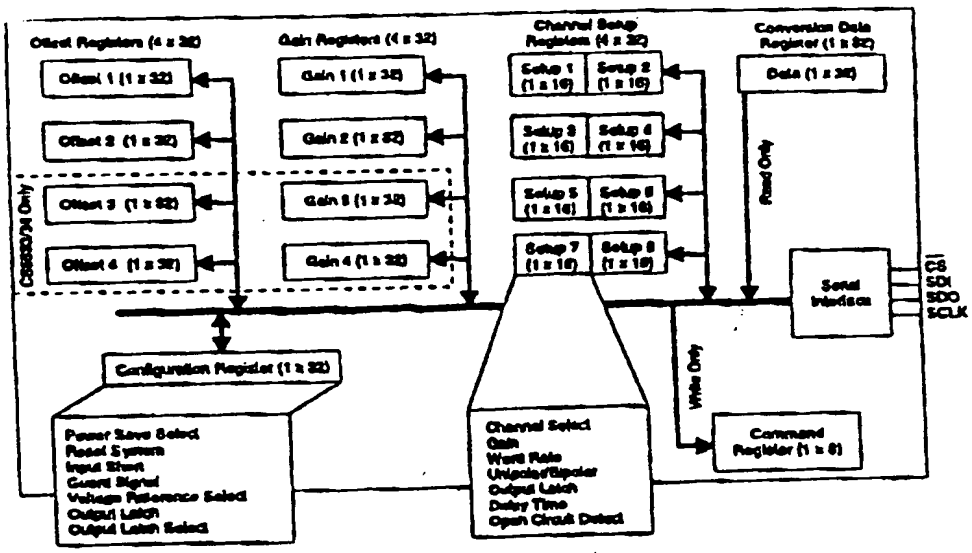

Offset Registers (4 x 32)
Offset 1 (1 x 32)
Offset 2 (1 x 32)
Offset 3 (1 x 32)
Offset 4 (1 x 32)
Gain Registers (4 x 32)
Gain 1 (1 x 32)
Gain 2 (1 x 32)
Gain 3 (1 x 32)
Gain 4 (1 x 32)
Channel Setup Registers (4 x 32)
Setup 1 (1 x 16)
Setup 2 (1 x 16)
Setup 3 (1 x 16)
Setup 4 (1 x 16)
Setup 5 (1 x 16)
Setup 6 (1 x 16)
Setup 7 (1 x 16)
Setup 8 (1 x 16)
Conversion Data Register (1 x 32)
Data (1 x 32)
Read Only
Write Only
Serial Interface
CS
SDI
SDO
SCLK
Configuration Register (1 x 32)
Power Save Select
Reset System
Input Short
Guard Signal
Voltage Reference Select
Output Latch
Output Latch Select
Channel Select
Gain
Word Rate
Unipolar/Bipolar
Output Latch
Delay Time
Open Circuit Detect
Command Register (1 x 8)

FIGURE 4.1

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	ARA	CS1	CS0	R/$\overline{W}$	RSB2	RSB1	RSB0

BIT	NAME	VALUE	FUNCTION
D7	Command Bit, C	0	Must be logic 0 for these commands.
		1	These commands are invalid if this bit is logic 1.
D6	Access Registers as Arrays, ARA	0	Ignore this function.
		1	Access the respective registers, offset, gain, or channel-setup, as an array of registers. The particular registers accessed are determined by the RS bits. The registers are accessed MSB first with physical channel 0 accessed first followed by physical channel 1 next and so forth.
D5-D4	Channel Select Bits, CS1-CS0	00	CS1-CS0 provide the address of one of the two (four for CS5533/34) physical input channels. These bits are also used to access the calibration registers associated with the respective physical input channel. Note that these bits are ignored when reading data register.
		01	
		10	
		11	
D3	Read/$\overline{\text{Write}}$, R/$\overline{W}$	0	Write to selected register.
		1	Read from selected register.
D2-D0	Register Select Bit, RSB3-RSB0	000	Reserved
		001	Offset Register
		010	Gain Register
		011	Configuration Register
		100	Conversion Data Register (Read Only)
		101	Channel-Setup Registers
		110	Reserved
		111	Reserved

FIGURE 4.2

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	MC	CSRP2	CSRP1	CSRP0	CC2	CC1	CC0

BIT	NAME	VALUE	FUNCTION
D7	Command Bit, C	0	These commands are invalid if this bit is logic 0.
		1	Must be logic 1 for these commands.
D6	Multiple Conversions, MC	0	Perform fully settled single conversions.
		1	Perform conversions continuously.
D5-D3	Channel-Setup Register Pointer Bits, CSRP	000 ... 111	These bits are used as pointers to the Channel-Setup registers. Either a single conversion or continuous conversions are performed on the channel setup register pointed to by these bits.
D2-D0	Conversion/Calibration Bits, CC2-CC0	000	Normal Conversion
		001	Self-Offset Calibration
		010	Self-Gain Calibration
		011	Reserved
		100	Reserved
		101	System-Offset Calibration
		110	System-Gain Calibration
		111	Reserved

FIGURE 4.3

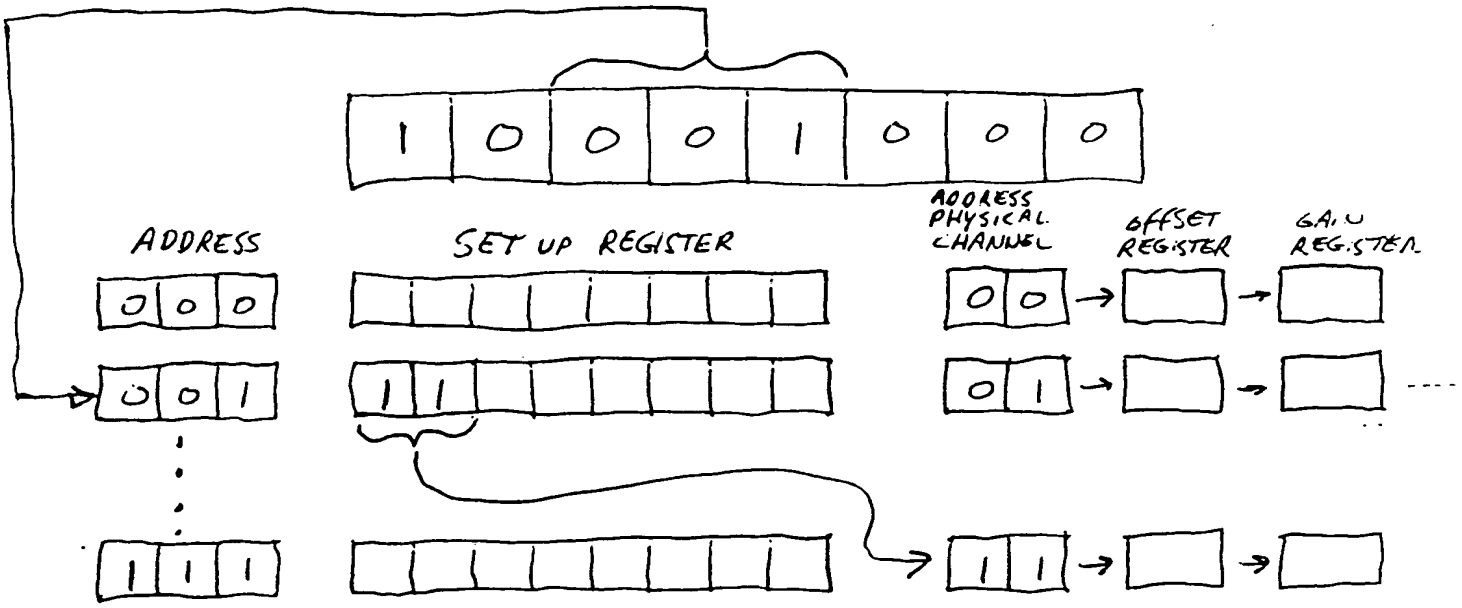

1 0 0 0 1 0 0 0
ADDRESS
SET UP REGISTER
ADDRESS PHYSICAL CHANNEL
OFFSET REGISTER
GAIN REGISTER
0 0 0
0 0 1
1 1 1
0 0
0 1
1 1

FIGURE 4.4

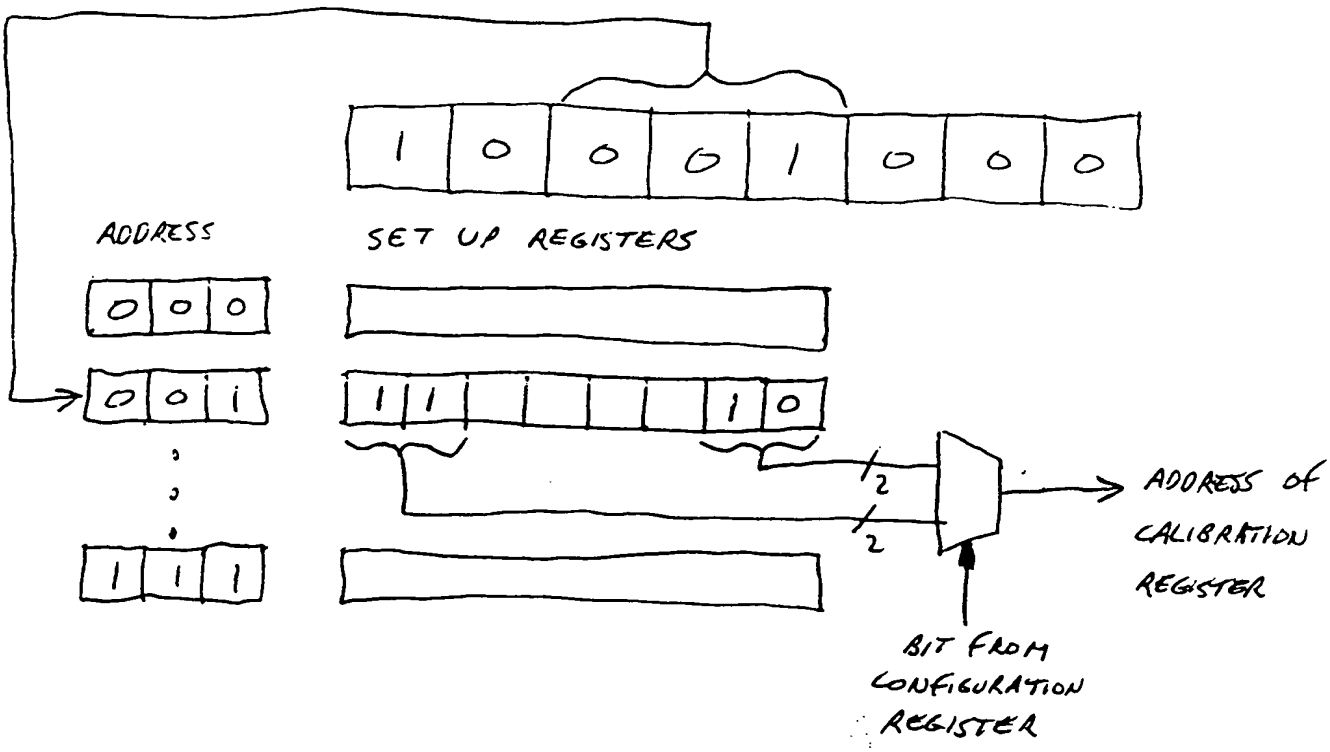

1 0 0 0 1 0 0 0
ADDRESS
SET UP REGISTERS
0 0 0
0 0 1
1 1 1
1 1
1 0
1/2
1/2
ADDRESS OF CALIBRATION REGISTER
BIT FROM CONFIGURATION REGISTER

FIGURE 4.5

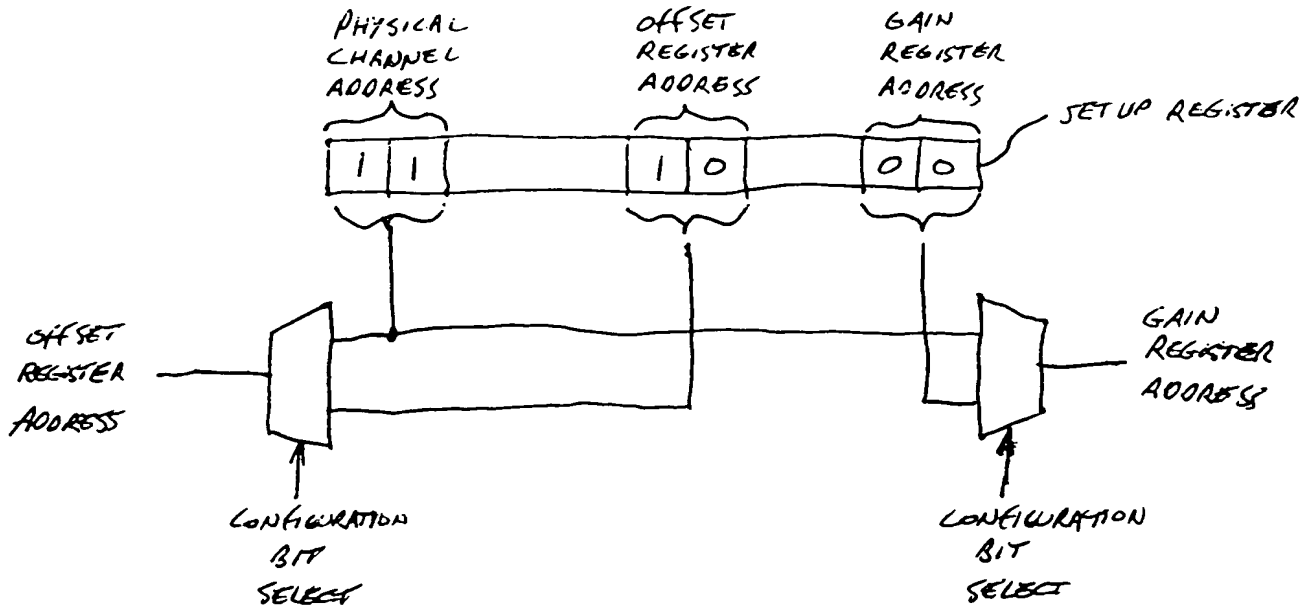

PHYSICAL CHANNEL ADDRESS
OFFSET REGISTER ADDRESS
GAIN REGISTER ADDRESS
SET UP REGISTER
1 1
1 0
0 0
OFFSET REGISTER ADDRESS
GAIN REGISTER ADDRESS
CONFIGURATION BIT SELECT
CONFIGURATION BIT SELECT

FIGURE 4.6

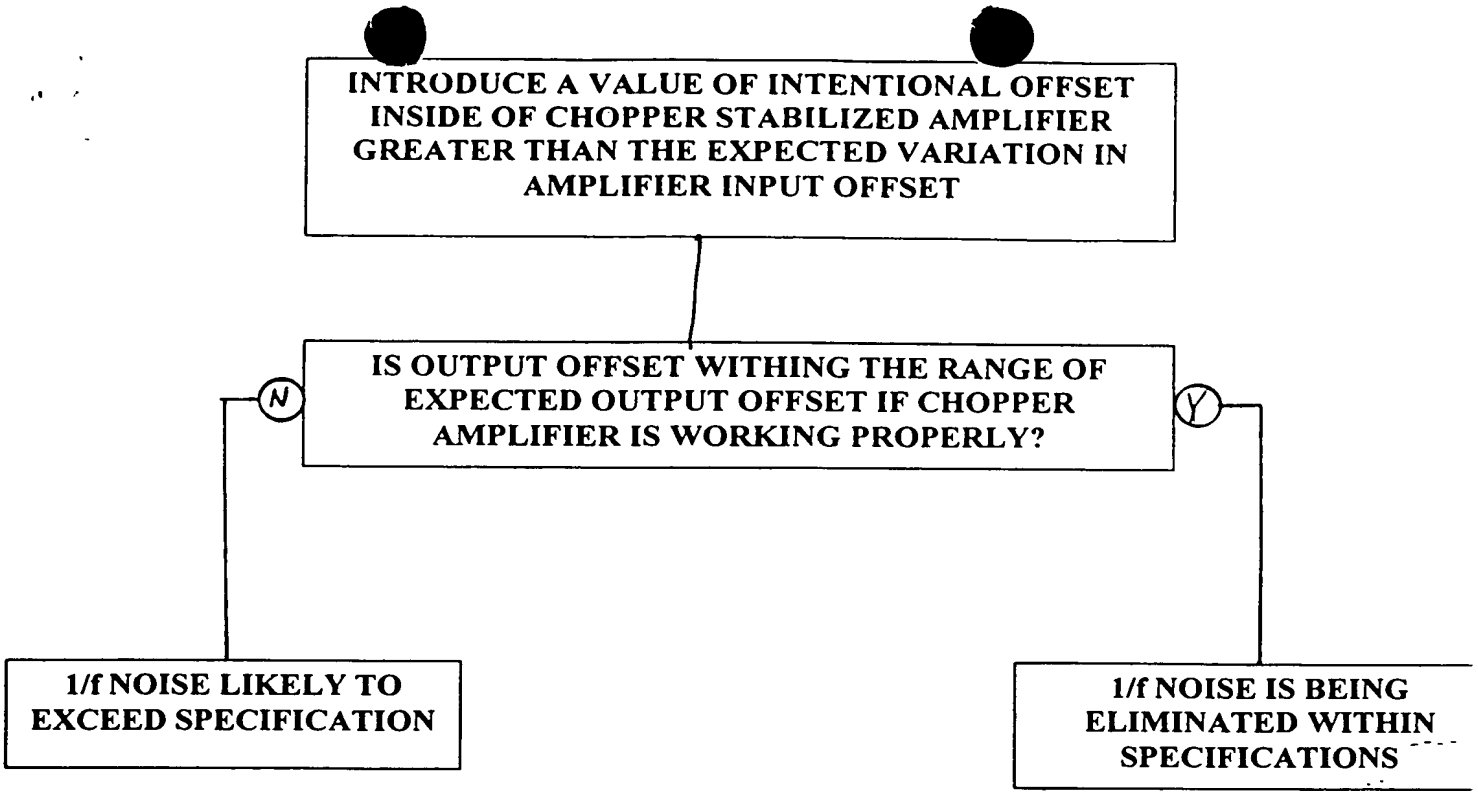


FIGURE 5.1

Thermocouple Application

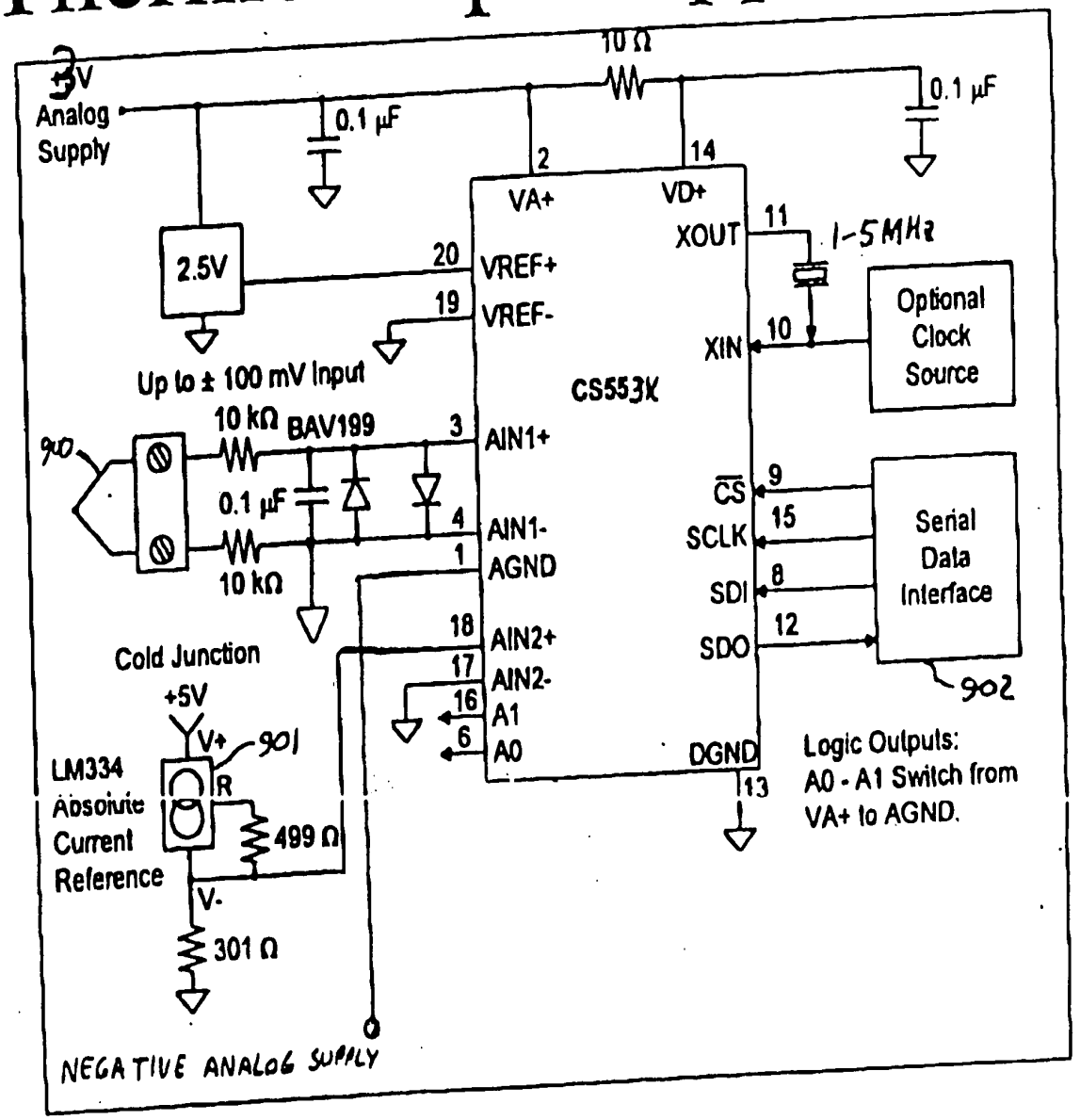


FIGURE 6.1

Bridge Transducer Application

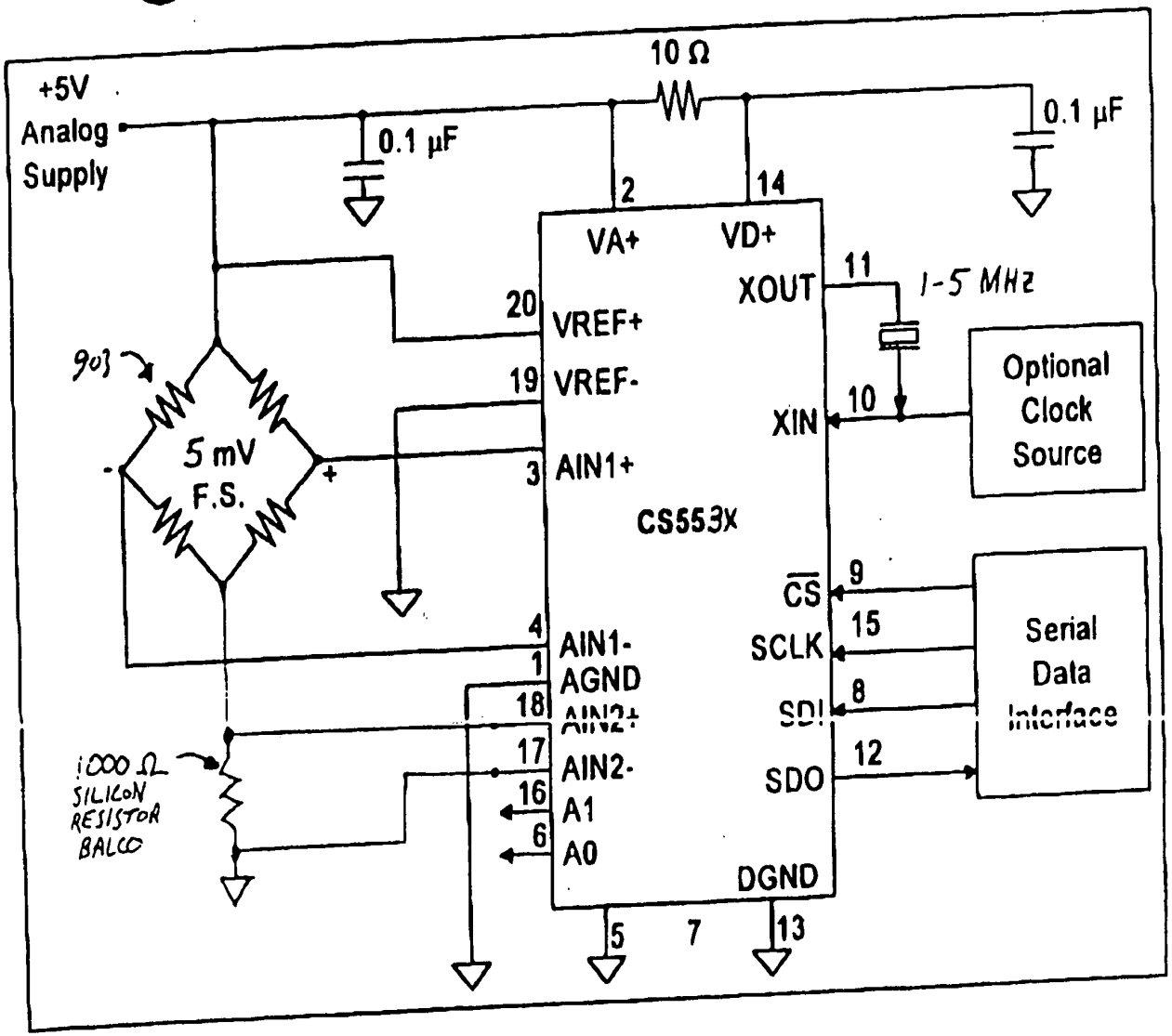


FIGURE 6.2